Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-46. (Canceled).

47. (Previously Presented) An optical logic circuit performing an inversion function, comprising:

a semiconductor substrate comprising a first semiconductor material;

a first semiconductor light source formed on the semiconductor substrate using integrated circuit processing techniques;

a second semiconductor light source formed on the semiconductor substrate using integrated circuit processing techniques;

an optical layer overlaying the semiconductor substrate, the optical layer comprising a second semiconductor material, the optical layer configured to provide a plurality of optical pathways, wherein the pathways are formed using integrated circuit processing techniques, the optical pathways forming an optical logic gate, the optical logic gate having a first optical input coupled to the first semiconductor light source formed on the same semiconductor substrate and configured to receive a first light input signal directly from the first semiconductor light source, a second optical input coupled to the second semiconductor light source formed on the same semiconductor substrate and configured to receive a second light input signal directly from the second semiconductor light source, wherein the first light input signal is a constant coherent signal and the second light input signal is a coherent signal which can be selectively turned on and off, an interference region coupled to the first and second optical inputs and configured to receive the first light input signal from the first optical input and the second light input signal from the second optical input, and an optical output coupled to the interference region opposite the first and second optical inputs;

the interference region comprises the second semiconductor material and is

bounded on all sides by semiconductor material other than the second semiconductor material except where the first and second optical inputs and optical output are located, wherein the interference region is a uniform three dimensional region and contains no potential barriers partitioning the interference region between the first and second optical inputs and the optical output, the first and second optical inputs are spaced apart and the optical output is positioned along a chosen line, along which maximum destructive interference occurs when the second light input signal at the second optical input is on, the maximum destructive interference being caused exclusively by the interaction between first and second light input signals, wherein an output light signal is a Boolean logic output signal based on the second light input signal, the output light signal exits the interference region at the optical output, the output light signal having one of two intensities, either a substantially on or a substantially off intensity.

48. (Previously Presented) The optical logic circuit of claim 47, wherein the interference region is configured to cause substantial cancellation of light exiting the interference region through the optical output when the second light input to the second optical input is turned on.

49. (Previously Presented) The optical logic circuit of claim 47, further comprising a third semiconductor light source formed on the semiconductor substrate, wherein the interference region includes a third optical input coupled to the third semiconductor light source formed on the same semiconductor substrate and configured to receive a third light input signal directly from the third semiconductor light source, wherein the third light input signal is a coherent signal which can be selectively turned on and off.

50. (Previously Presented) The optical logic circuit of claim 49, wherein the interference region is configured to cause substantial cancellation of light exiting the interference region through the optical output when the second light input signal is provided to the interference region through the second optical input and the third light input signal is provided to the interference region through the third optical input.

51. (Previously Presented) The optical logic circuit of claim 47, wherein the Boolean logic output is a NOT (inverter) function.

52. (Previously Presented) The optical logic circuit of claim 49, wherein the Boolean logic output is a NOT AND (NAND) function.

53. (Previously Presented) The optical logic circuit of claim 47, wherein the integrated circuit processing techniques include at least one of photoresist techniques, etching techniques and deposition techniques.

54. (Previously Presented) The optical logic circuit of claim 52, having a multiplicity of optical pathways and interference regions configured to function as an optical processor, wherein the optical processor comprises NOT (inverter) gates and NOT AND (NAND) gates.

55. (Previously Presented) An optical logic gate performing an inversion function for an optical processor, comprising:

a semiconductor substrate comprises a first semiconductor material;

a patterned optical layer overlaying the semiconductor substrate, wherein the patterned optical layer is formed using integrated circuit processing techniques, the optical layer comprising a second semiconductor material, the patterned optical layer comprising an interference region coupled to a first optical conduit and a second optical conduit formed of the second semiconductor material, the first optical conduit coupled to a first semiconductor light source and configured to receive a first light input signal directly from the first semiconductor light source formed on the same semiconductor substrate, and the second optical conduit coupled to a second semiconductor light source and configured to receive a second light input signal directly from the second semiconductor light source formed on the same semiconductor substrate, wherein the first light input signal is a constant coherent light and the second light input signal is a coherent light that may be selectively turned on and off, wherein the first and second semiconductor light sources are formed using integrated circuit processing techniques; and

the interference region coupled to the first optical conduit and configured to receive the first light input signal from the first optical conduit, the interference region coupled to the second optical conduit and configured to receive the second light input signal from the second optical conduit, a predetermined axis in the interference region along which maximum interference of the first and second optical input signals in the interference region occurs, the interference region is coupled to a third optical conduit configured to provide an optical output signal, wherein the third optical conduit is configured to align with the predetermined axis, the maximum destructive interference being caused exclusively by the interaction between first and second light input signals,

wherein the interference region is formed of the second semiconductor material and bounded on all sides by semiconductor material other than the second semiconductor material except where the first, second and third optical conduits are coupled to the interference region, wherein the interference region is a uniform three dimensional region and contains no potential barriers partitioning the interference region between the first and second optical conduits and the third optical conduit, wherein the optical output signal is a Boolean logic output signal based on the second light input signal that may selectively be turned on and off, the output signal having one of two intensities, either a substantially on or a substantially off intensity.

56. (Previously Presented) The optical logic gate of claim 55, wherein the optical logic gate provides a Boolean NOT function as output.

57. (Previously Presented) The optical logic gate of claim 55, further comprising:

a fourth optical conduit coupled to the interference region and configured to receive a third light input signal directly from a third semiconductor light source formed on the semiconductor substrate.

58. (Previously Presented) The optical logic gate of claim 57, wherein the optical logic gate provides a Boolean NOT AND (NAND) function as output.

59. (Previously Presented) The optical logic gate of claim 55, wherein the first semiconductor material comprises at least one of silicon (Si) and Gallium Arsenide (GaAs).

60. (Previously Presented) The optical logic gate of claim 55, wherein the second semiconductor material comprises doped semiconductor material.

61. (Previously Presented) The optical logic gate of claim 55, further comprising:

an electromagnetic detector formed on the semiconductor substrate and coupled to the third optical conduit and configured to convert the optical output signal into an electrical signal.

62. (Canceled).

63. (Previously Presented) The optical logic gate of claim 55, wherein the first semiconductor light source and the second semiconductor light source are Laser diodes.

64. (Previously Presented) The optical logic gate of claim 55, wherein first semiconductor light source and the second semiconductor light source are semiconductor diodes.

65.-78. (Canceled).

79. (Currently Amended) An optical logic circuit performing an inversion function, comprising:

a semiconductor substrate comprising a first semiconductor material;

a first semiconductor light source formed on the semiconductor substrate using integrated circuit processing techniques;

a second semiconductor light source formed on the semiconductor substrate using integrated circuit processing techniques;

an optical layer overlaying the semiconductor substrate, the optical layer comprising a second semiconductor material, the optical layer configured to provide a plurality of optical pathways, wherein the optical pathways are formed using integrated circuit processing

techniques, the optical pathways forming an optical logic gate, the optical logic gate comprising:

a first optical input pathway coupled to the first semiconductor light source formed on the same semiconductor substrate and configured to receive a first light input signal directly from the first semiconductor light source,

a second optical input pathway coupled to the second semiconductor light source formed on the same semiconductor substrate and configured to receive a second light input signal directly from the second semiconductor light source, wherein the first light input signal and the second light input signal are coherent signals which may be selectively turned on and off, wherein the first and second optical input pathways are in parallel,

an interference region coupled to the first and second optical input pathways and configured to receive the first light input signal from the first optical input pathway and the second light input signal from the second optical input pathway, and

a first optical output pathway coupled to the interference region opposite the first and second optical input pathways;

wherein the interference region comprises the second semiconductor material and is bounded on all sides by semiconductor material other than the second semiconductor material except where the first and second optical input pathways and first optical output pathways are coupled to the interference region, wherein the interference region is a uniform three dimensional region and contains no potential barriers partitioning the interference region between the first and second optical input pathways and the first optical output pathway, the first and second optical input pathways are spaced apart and the first optical output pathway is positioned along a chosen line, along which maximum destructive interference occurs when the first and second light input signals are both on, the maximum destructive interference being caused exclusively by the interaction between first and second light input signals, wherein an output light signal is a first Boolean logic output signal having a logic low when the first and second light input signals are both on, and a logic high when only one of the light input signals is on, wherein the output logic signal is the logic low when the output light signal has a substantially off intensity and the output logic signal is the logic high when the output light signal has a substantially [[no]] <u>on</u> intensity.

80. (Previously Presented) The optical logic circuit of claim 79, wherein the first and the second light input signals are selectively turned on and off, wherein the first Boolean logic output is an XOR (exclusive OR) function.

81. (Currently Amended) The optical logic circuit of claim 79, wherein the first light input signal [[is]] stays on constantly and the second light input signal is selectively turned on and off, wherein the first Boolean logic output is a NOT (inverter) function.

82. (Previously Presented) The optical logic circuit of claim 79, further comprising:

a third semiconductor light source formed on the semiconductor substrate using integrated circuit processing techniques, wherein the optical layer further comprises a third optical input pathway coupled to the interference region and to the third semiconductor light source formed on the same semiconductor substrate, the third optical input pathway being configured to receive a third light input signal directly from the third semiconductor light source, wherein the third light input signal is a constant coherent signal, wherein the first Boolean logic output is a NOT AND (NAND) function.

83. (Previously Presented) The optical logic circuit of claim 82, wherein the interference region is a first interference region and the optical output pathway is a first optical output pathway, the optical logic circuit further comprising:

a second interference region coupled to the first interference region via the first optical output pathway and configured to receive the output light signal as a fourth light input signal that can be selectively turned on and off based on the interference of the first, second and third light input signals in the first interference region;

a fourth optical input pathway coupled to a fourth semiconductor light source formed on the same semiconductor substrate and configured to receive a fifth light input signal directly from the fourth semiconductor light source, wherein the fifth light input signal is a constant coherent signal, wherein the second interference region is coupled to the fourth optical input pathway and configured to receive the fifth light input signal from the fourth optical pathway;

a second optical output pathway coupled to the second interference region opposite the first output optical pathway and fourth optical input pathway;

wherein the second interference region comprises the second semiconductor material and is bounded on all sides by semiconductor material other than the second semiconductor material except where the first optical output pathway, the fourth optical input pathway and the second optical output pathway are coupled to the second interference region, wherein the second interference region is a uniform three dimensional region and contains no potential barriers partitioning the second interference region between the first optical output pathway, the fourth optical input pathway and the second optical output pathway, the first optical output pathway and the fourth optical input pathway are spaced apart and the second optical output pathway is positioned along a chosen line, along which maximum destructive interference occurs when the fourth and fifth light input signals are both on, the maximum destructive interference being caused exclusively by the interaction between fourth and fifth light input signals, wherein a second output light signal is a second Boolean logic output signal having a logic low when the fourth light input signal is on, and a logic high fourth light input signal is off, wherein the Boolean logic output of the optical logic circuit is an AND function.

84. (Previously Presented) The optical logic circuit of claim 83, wherein the third semiconductor light source and the fourth semiconductor light source are the same light source.

85. (Previously Presented) The optical logic circuit of claim 79, wherein the first and second light sources are semiconductor lasers comprising $Al_xGa_{1-x}As_ySb_{1-y}$.

86. (Previously Presented) The optical logic circuit of claim 79, wherein the first and second light sources are semiconductor lasers comprising $Ga_xIn_{1-x}As_yP_{1-y}$.

87. (Previously Presented) The optical logic circuit of claim 79, wherein the second semiconductor material is doped semiconductor material.

88. (Previously Presented) The optical logic circuit of claim 79, further comprising:

an electromagnetic detector formed on the semiconductor substrate and coupled to the first optical output pathway and configured to convert the first output light signal into an electrical signal.

89. (Previously Presented) The optical logic circuit of claim 47, further comprising:

an electromagnetic detector formed on the semiconductor substrate and coupled to the optical output of the interference region and configured to convert the output light signal into an electrical signal.

90. (Previously Presented) A method of forming an optical logic circuit configured to perform an inversion function, comprising:

providing a semiconductor substrate, wherein the substrate is a first semiconductor material;

depositing a second semiconductor material above the semiconductor substrate to form an optical layer;

etching the optical layer in accordance with a pattern to form a plurality of optical pathways, the plurality of optical pathways forming an optical logic gate, the optical logic gate comprising an interference region, a first optical input pathway coupled to the interference region and configured to receive a first light input signal directly from a first semiconductor light source, a second optical input pathway coupled to the interference region and configured to receive a second light input signal directly from a second semiconductor light source, an optical output pathway coupled to the interference region opposite the first and second optical input pathways, wherein the interference region is configured to receive the first light input signal from the first optical input pathway and the second light input signal from the second optical input pathway, wherein the first and second optical input pathways are in parallel, wherein the interference region is a uniform three dimensional region and contains no potential barriers partitioning the interference region between the first and second optical input pathways and the optical output pathway, wherein the first and second optical input pathways are spaced apart and

the optical output pathway is positioned along a chosen line, along which maximum destructive interference occurs when the first and second light input signals are provided, the maximum destructive interference being caused exclusively by the interaction between the first and second light input signals, wherein an output light signal is a Boolean logic output signal based on the first and second light input signals, the output light signal exits the interference region at the optical output pathway, the output light signal having one of two intensities, either a substantially on or a substantially off intensity; and

depositing a third semiconductor layer above the etched optical layer and the substrate, wherein the third semiconductor layer is a non-translucent semiconductor layer.

91. (Previously Presented) The method of claim 90, wherein the first and second semiconductor light sources are formed on the same semiconductor substrate as the optical logic gate.

92. (Previously Presented) The method of claim 91, wherein the optical layer of the logic gate also forms the junction layer of the first and second semiconductor light sources.

93. (Previously Presented) The method of claim 92, wherein the junction layer of the first and second semiconductor light sources is etched in accordance with the pattern to coupled to the first and second optical input pathways, respectively.